Features and Benefits

- 3-Axis Electronic Magnetometer
- Cost effective and compact solution
- Factory set full scale range
  Max ±48 gauss selectable
- On chip EEPROM trimming
- Operating temp range:- 40℃ to 85℃
- 1.8V compatible IO
- 16 bits ADC
- Fast mode IIC serial interface
- Interrupt supported
- RoHS compliant

Applications

- Electronic Compass
- Smartphone
- Tablet PC
- Handheld devices

General Description

The ST480MC-A is an integrated 3-axis magnetometer with signal processing circuitry and integrated IIC interface. It provides excellent temperature stability and high resolution over the whole operating temperature range (-40℃ ~ 85℃).

The ST480MC-A has ±48 gauss Full Scale Range to provide multi-domain application.

The ST480MC-A delivers output signal proportional to magnetic field it measures on each axis. Meanwhile, it provides an IIC digital output. Factory trimmed scale factors eliminate the need for external active components and end-user calibration.

The ST480MC-A is packaged in WL-CSP package.

Order Information

Model Name	Full Scale Range	Package Description
ST480MC-A	±48 gauss	8pin WL-CSP, 1.28*1.28*0.5mm^3

Content

1. Functional Diagram

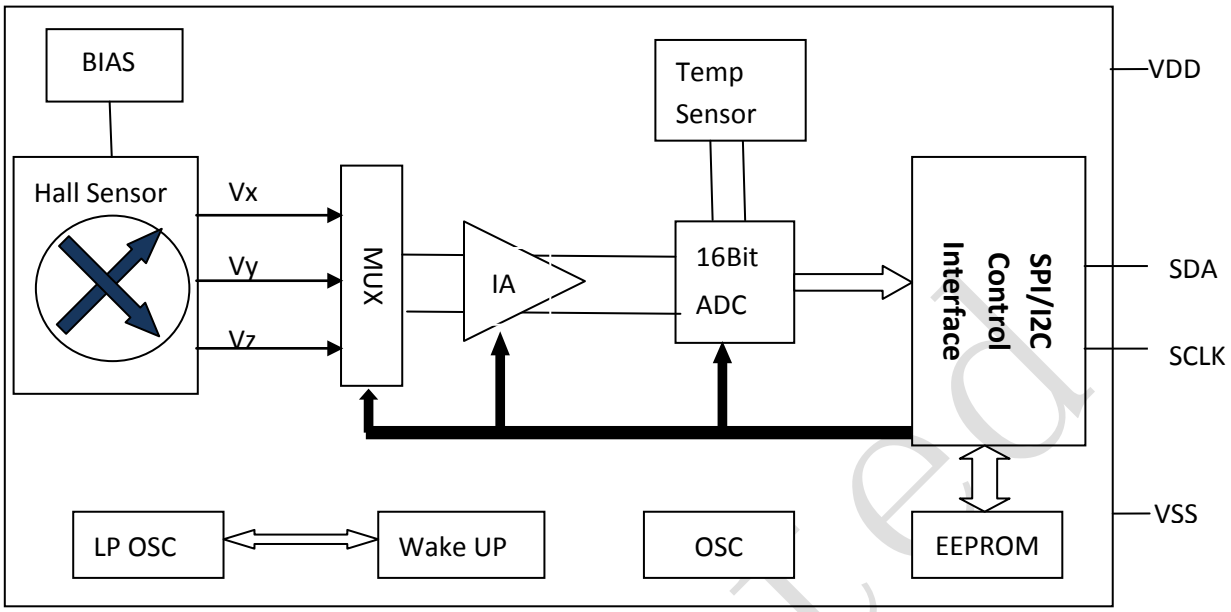


Figure 1: Function block diagram

2. Sensor Specifications

DC Operating Parameters T=-40℃ to 85℃, Vdd=2.2V to 3.6V (unless otherwise specified)
All parameters are specified @ Vdd=3.0V and T=25℃

Parameter	Conditions	Min.	Typ.	Max.	Unit
Full Range	Each axis		±48		gauss
Non Linearity	±48gauss		0.1		% of FS
Sensitivity	Z axis		400		LSBs/Gauss
	X and Y axis		667		LSBs/Gauss
Magnetic Resolution	Z axis X and Y axis		2.5 1.5		*mG/LSB* *mG/LSB*
T_{CONV}	From idle to data ready	1		256	mS
T_{STBY}	From IDLE to STBY		250		µS
T_{ACTIVE}	From STBY to ACTIVE		8		µS
$T_{INTERVAL}$	Time in between 2 conversions(Burst mode or Wake-up on Change)	20		5000	mS
T_{POR}	Power-on-reset completion time		0.6	1.5	ms
T_{CONVM}	Single Magnetic axis conversion time(1) typical programming range	0.192		66.56	ms
		$[(2+2^{\wedge DIG\_FILT})*2^{\wedge OSR}*0.064]$			
T_{CONVT}	Temperature conversion time typical programming range	0.192		1.54	ms
		$[2^{\wedge OSR2}*0.192]$			
T_{CONV_SMM}	Total conversion time in Single Measurement Mode(1)	$T_{STBY} + T_{ACTIVE} + m*T_{CONVM} + T_{CONVT}$			ms
$T_{CONV\_BURSTWOC}$	Total conversion time in BURST or WOC Mode(1)	$T_{ACTIVE} + m*T_{CONVM} + T_{CONVT}$			ms

(1) This conversion time is defined as the time to acquire a single axis of the magnetic flux density. When measuring multiple axes, they are obtained through time-multiplexing, i.e. X(t), Y(t+T_{CONVM}) and Z(t+2*T_{CONVM}). The conversion time is programmable through parameters OSR and DIG_FILT for magnetic conversion time and OSR_2 for temperature conversion time.

(2) The time $T_{INTERVAL}$ is defined as the time between the end of one set of measurements (any combination of TXYZ) and the start of the following same set of measurements in BURST and

WOC mode.

3. Electrical Characteristics

Electrical characteristics @ Vdd=3.0V, T=25℃ unless otherwise noted

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply		2.2	3	3.6	V
VLOGIC	Digital IO power supply		1.65	1.8	VDD	V
$I_{DD,\ CONV}$	Conversion Current			2.4	3.5	mA
$I_{DD,\ STBY}$	Standby Current			80		μA
$I_{DD,\ IDLE}$	Idle current			1	2	μA
$I_{DD,\ NOM}$	Nominal Current	Data-rate =10Hz, t_{CONV}=16mS		0.4		mA

4. Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Parameter	Min	Max	Unit
Operating supply voltage	-0.3	6	V
Operating Temperature	-40	85	℃
Storage Temperature Range	-50	125	℃
ESD(HBM)		2000	V

5. Pin Order and Pin Description

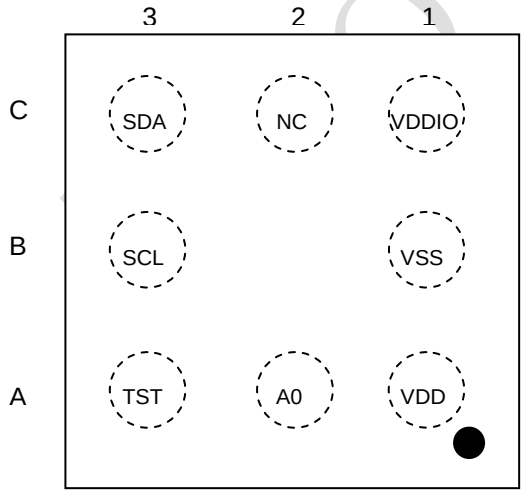


Figure 5.1: PIN order for ST480MC-A Top view WL-CSP 8pin 1.28 x 1.28 x 0.5 mm^3

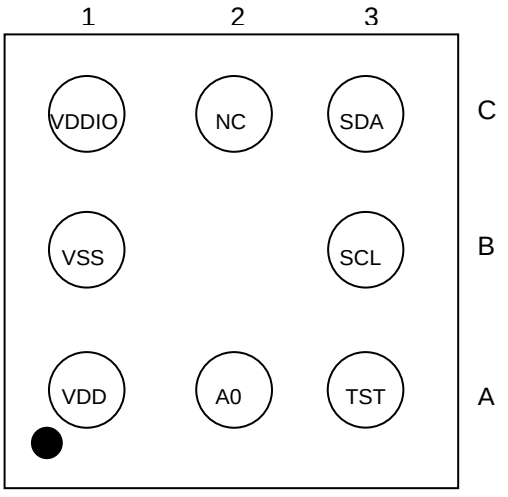


Figure 5.2: ST480MC-A Bottom view

Table PIN Description

PIN No. ST480MC-A	PIN Name	PIN Function
A1	VDD	Positive power supply pin.
A2	A0	LSB of 7bits IIC address; Do not float
A3	TST	Test pin Pulled down by 100kΩ internal resister. Keep this pin electrically non-connected.
B1	VSS	Ground pin.
B3	SCL	Control data clock input pin Input: Schmidt trigger
C1	VDDIO	Digital interface positive power supply pin
C2	NC	No Connected
C3	SDA	I2C serial data input/output pin

6. Functional Explanation

6.1 Magnetic Sensor

The measurement data increases as the magnetic flux density increases in the arrow directions.

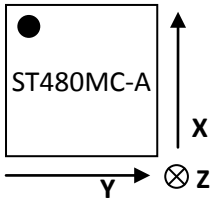


Figure 6.1: Sensor Direction of ST480MC-A

6.2 The noise of sensor

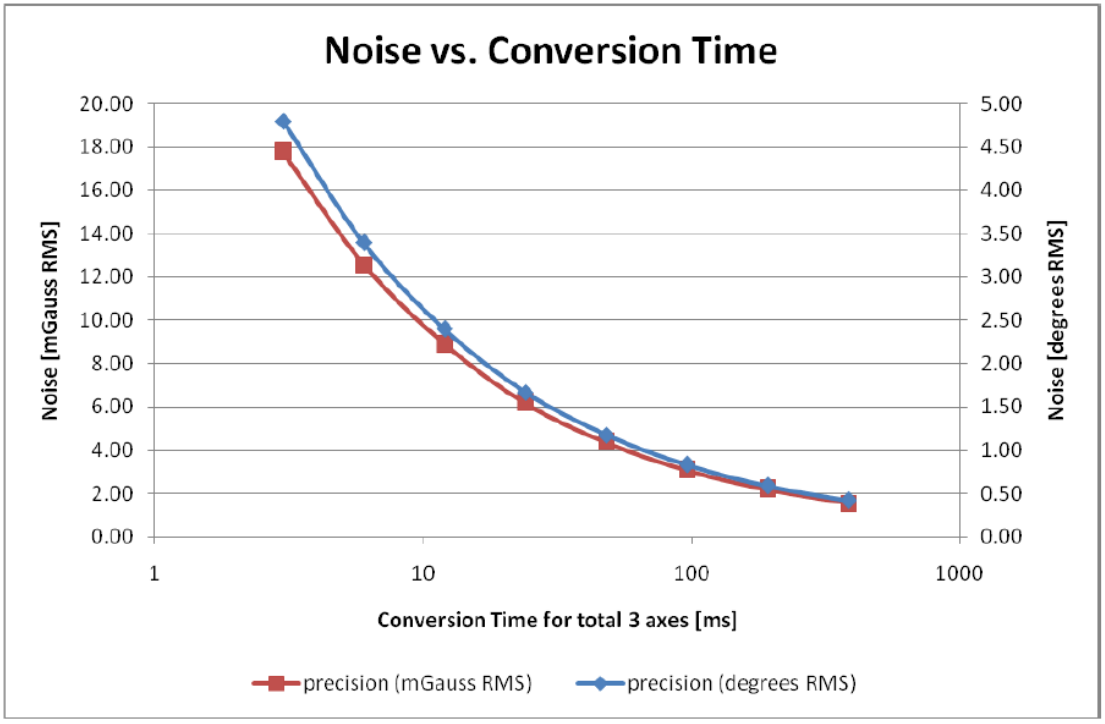


Figure 6.2: Relation between the noise and conversion time

6.3 Operation mode

The ST480MC-A can operate in 3 modes: single measurement mode, burst mode, wakeup mode. The statement changed should follow the state diagram

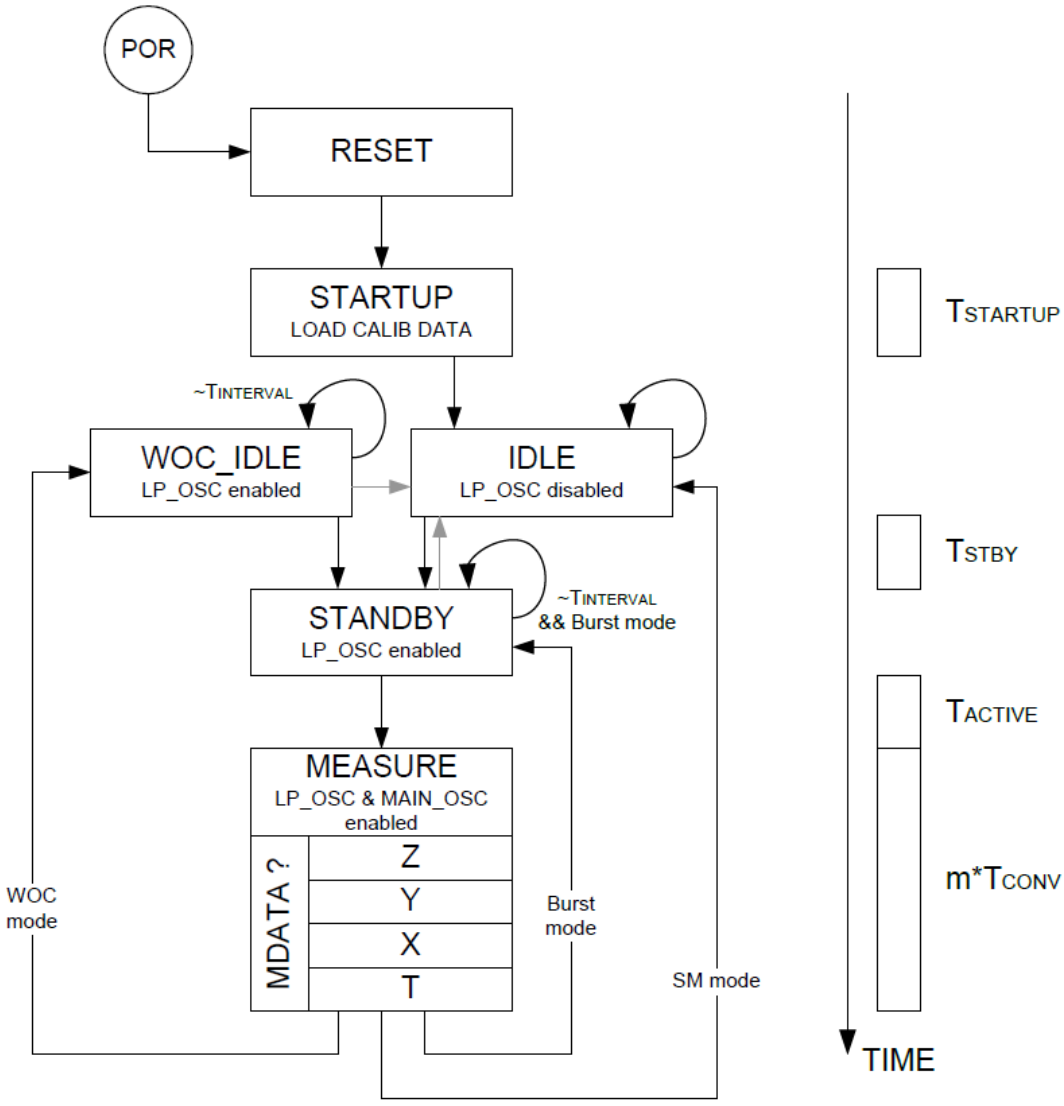


Figure 6.3: Top-Level State Diagram with indication of timings

- Single measurement mode

  The master will ask for data via the corresponding protocol (I2C or SPI), waking up the ASIC to make a single conversion, immediately followed by an automatic return to sleep mode (IDLE) until the next polling of the master. This polling can also be done by strobing the TRG pin, which has the same effect as sending a protocol command for a single measurement.

  Whenever the sensor is set to this mode (or after startup) the ST480MC-A goes to the IDLE state where it awaits a command from the master to perform a certain acquisition. The duration of the acquisition will be the concatenation of the T_{STBY}, T_{ACTIVE} and $m*T_{CONV}$ (with m # of axes). The conversion time will effectively be programmable by the user, but is equally a function of the required axes/temperature to be measured. Upon reception of such a polling command from the master, the sensor will make the necessary

acquisitions, and set the INT/DRDY pin high to signal that the measurement has been performed and the master can read out the data on the bus at his convenience. The INT/DRDY will be cleared either when:

- The master has issued a command to read out at least one of the measured components
- The master issues an Exit (EX) command to cancel the measurement
- The chip is reset, after POR (Power-on reset) or Reset command (RT)

- Burst mode:

  The ASIC will have a programmable data rate at which it will operate. This data rate implies auto-wakeup and sequencing of the ASIC, flagging that data is ready on a dedicated pin (INT). The maximum data rate will correspond to 1/3*T_{CONV} in case of 3 axes magnetic data. The time during which the ASIC has a counter running, but is not doing an actual conversion is called the Standby mode (STBY).

  When the sensor is operating in burst mode, it will make conversions at specific time intervals. The programmability of the user is the following:

  - Burst speed (TINTERVAL)
  - Conversion time (TCONV)
  - Axes/Temperature (MDATA)

  Whenever the ST480MC-A has made the selected conversions (based on MDATA), the DRDY pin will be set active H to indicate that the data is ready. It will remain high until the master has sent the command to read out at least one of the converted quantities (ZYXT). Should the master have failed to read out any of them by the time the sensor has made a new conversion, the DRDY pin will be strobed low for 10us, and the next rising edge will indicate a new set of data is ready.

- Wake-Up on Change:

  This mode is similar to the burst mode in the sense that the device will be auto-sequencing, with the difference that the measured component(s) is/are compared with a reference and in case the difference is bigger than a user-defined threshold, the INT pin is set. The user can select which axes and/or temperature fall under this cyclic check, and which thresholds are allowed.

  User can change the operating mode at all time through a specific command on the bus. The default start-up mode is Single Measurement mode (in IDLE state), but with a proper user command any mode can be set after power-up. Changing to Burst or WOC mode, coming from Single Measure mode is always accompanied by a measurement first. The top-level state diagram indicating the different modes and some relevant timing is shown below in Figure . In the Measure state, the MDATA flag will define which components will be measured (ZYXT). The sequential order cannot be modified by the user.

  The Wake-Up on Change (WOC) functionality can be set by the master with as main purpose to only receive an interrupt when a certain threshold is crossed. The WOC mode will

always compare a new burst value with a reference value in order to assess if the difference between both exceeds a user-defined threshold. The reference value is defined as one of the following:

- The first measurement of WOC mode is stored as reference value once, as a result of a measurement. This measurement at "t=0" is then the basis for comparison.
- The reference for acquisition (t) is always acquisition (t-1), in such a way that the INT/DRDY will only be set if the derivative of any component exceeds a threshold.

The in-application programmability is the same as for burst mode, but now the thresholds for setting the interrupt are also programmable by the user, as well as the reference, if the latter is data(t=0) or data(t-1).

7. Serial Interface

7.1 Data Transfer protocol

The supported protocols are I2C and SPI. The SENB/CS pin (pin #2 in QFN package) is used to define the protocol to be used:

- /CS = 0 for SPI, addressing the ST480MC-A slave in SPI mode (3- and 4-wire)
- /CS = 1 for I2C, addressing the ST480MC-A slave when the correct address is transmitted over the bus

To make sure the activity on the SPI bus can't be accidentally interpreted as I2C protocol, programming bits are available in the EEPROM of the ST480MC-A to select the protocol. It concerns the COMM_MODE[1:0] bits with the following effect:

COMM_MODE[1]	COMM_MODE[0]	Description
0	X	The mode in which the first valid command is transmitted to the ST480MC-A defines the operating mode (SPI or I2C) for all its future commands, until a reset (hard or soft) is done.
1	0	SPI mode only
1	1	I2C mode only

7.1.1 I2C Protocol

Slave Address

The ST480MC-A always work as a slave device. The I2C address is made up of some memory written value and hard-coded bits as follows: I2C_ADDR[7:0] = {EE_I2C_ADDR[4:0],A_1,A_0,R/W} with A_i the user-selectable active-high value of the input pads of the ST480MC-A, referred to the V_{DD} supply system and EE_I2C_ADDR[4:0] default programmed to 03h. When the R/W bit is set to"1", READ instruction is executed. When the R/W bit is set to"0", WRITE instruction is executed.

Table1: for ST480MC-A (8pin WL-CSP):

MSB							LSB
0	0	0	1	1	0	A0	R/W

Note: for ST480MC-A (8pin WL-CSP), A1 please connect to Gnd, for other package type A1 is second LSB of 7bits IIC address.

I2C Principle

The ST480MC-A supports I2C communication in both Standard Mode and Fast Mode. Bytes are transmitted MSB first, and in order to reconstruct words, the bytes need to be concatenated MSByte first. The general principle of communication is always the same:

1. Initiating the communication is always done by the Master (Start condition S)
2. Addressing the Slave (ST480MC-A) followed by a cleared bit to indicate the Master intends to write something to the specific addressed Slave
3. Acknowledging by the Slave if the transmitted address corresponds to the Slave's I2C address. If the latter isn't the case, any further activity on the bus except a Sr (Start Repeat) and P (Stop) condition will be ignored by the ST480MC-A
4. Sending a Command Byte by the Master, as depicted in Figure 5. The Slave will always acknowledge this, even if it is an unrecognized command.
5. Issuing a Start Repeat (Sr) condition by the Master in order to restart the addressing phase
6. Addressing the Slave (ST480MC-A) followed by a set bit to indicate the Master intends to read something from the specific addressed Slave
7. Acknowledging by the Slave if the transmitted address corresponds to the Slave's I^2C address. If the latter isn't the case, any further activity on the bus except a Sr (Start Repeat) and P (Stop) condition will be ignored by the ST480MC-A
8. Transmitting the Status Byte by the Slave, who is in control of the bus
9. Acknowledging by the Master if the data is well received
10. Generating a Stop condition (P) by the master

The Master controlled bus activity is shown in blue, the Slave controlled bus activity is shown in orange. In case a command is longer than a single byte, the bytes are transmitted sequentially before generating the Start Repeat (Sr) condition.

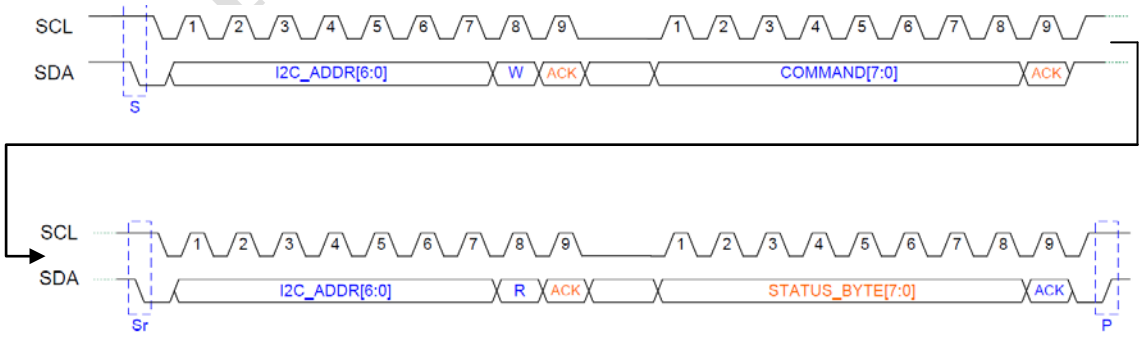


Figure 7.1 I2C slave protocol

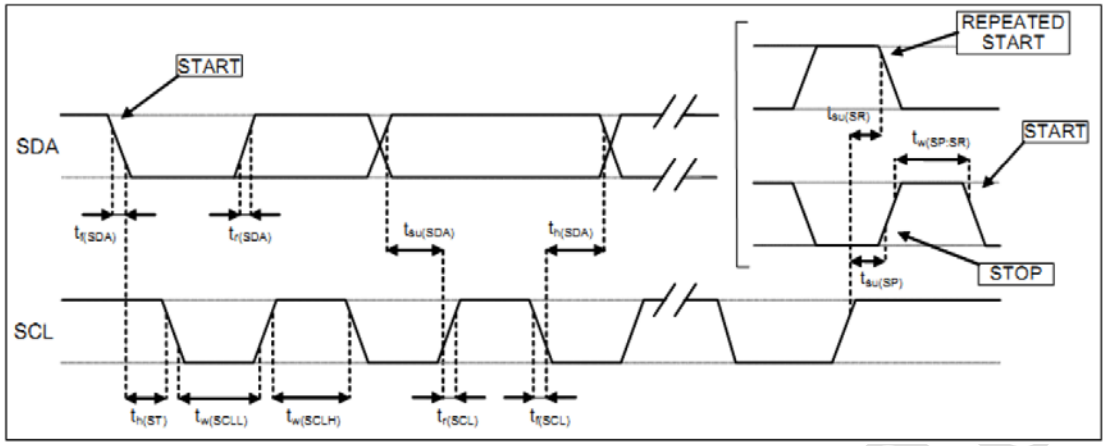


Figure 7.2 I2C slave timing diagram

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

Figure 7.3 I2C slave timing value

7.1.2 SPI Protocol

The ST480MC-A can handle SPI communication at a bitrate of 10Mhz. The SPI communication is implemented in a half-duplex way, showing high similarities with I2C communication, but addressing through the \CS (Chip Select) pin instead of through bus arbitration. The half-duplex nature is at the basis of the 3-wire SPI support. The implemented SPI mode is mode 3: CPHA=1 (data changed on leading edge and captured on trailing edge, and CPOL=1 (high level is inactive state). The Chip Select line is active-low.

Symbol	Parameter	Value (1)		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	10		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	5		
tdis(SO)	SDO output disable time		50	

Figure 7.4 SPI Timing Value

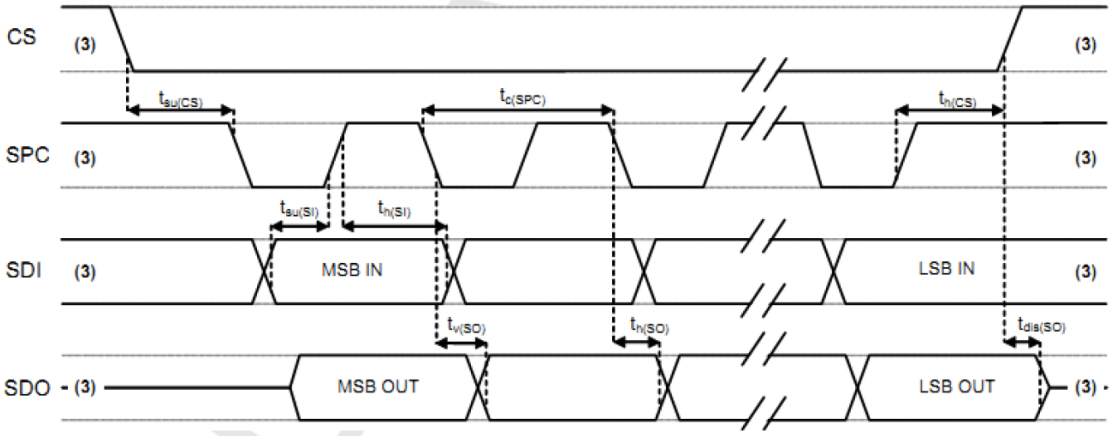


Figure 7.5 SPI Timing diagram

7.2 Register map

The ST480MC-A has ten 16bit Registers of non-volatile memory, and the same amount of volatile memory, The RR and WR commands impact the volatile memory only(yellow Area), there no direct access possible to the non-volatile memory.

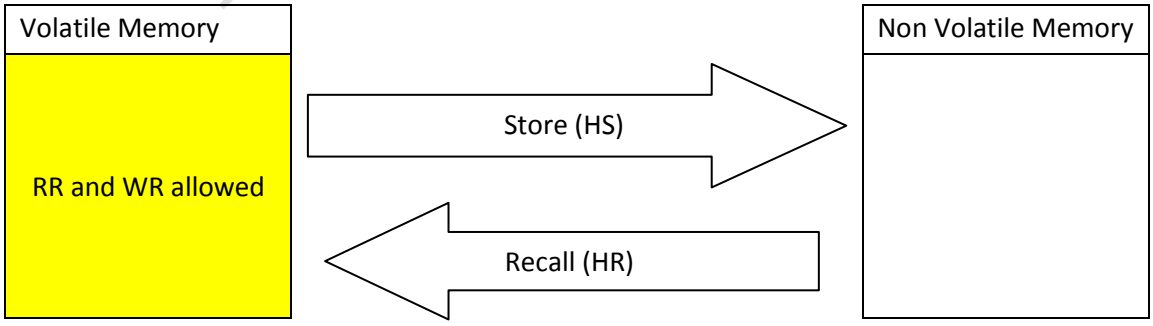


Figure 7.6 Memory Relationship

The Volatile memory map is given:

Address [7:2]	Bit Number															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	RESERVED_LOW							BIST	Zseries	Gain Sel			HALLCONF			
0x01	INT/TRIG	COMM_MODE		WOC_DIFF	EXT_TRIG	TCMP_EN	BURST_SEL (zyxt)			BURST_DATA_RATE						
0x02				OSR2			RES_XYZ					DIG_FILT			OSR	
0x03	SENS_TC_HT								SENS_TC_LT							
0x04	OFFSET_X															
0x05	OFFSET_Y															
0x06	OFFSET_Z															
0x07	WOXY_THRESHOLD															
0x08	WOZ_THRESHOLD															
0x09	WOT_THRESHOLD															

Table 7.1 Register Map

Note: Address[1:0] = 0x00

- RESERVED_LOW : Reserved IO trimming bits
- BIST : Enabled the on-chip coil, applying a Z-field [Built-In Self Test]
- Z_SERIES : Enable all plates for Z-measurement
- GAIN_SEL[2:0] : Analog chain gain setting, factor 5 between min and max code
- HALLCONF[3:0] : Hall plate spinning rate adjustment
- TRIG_INT_SEL : Puts TRIG_INT pin in TRIG mode when cleared, INT mode otherwise
- COMM_MODE[1:0] : Allow only SPI [10b], only I_2C [11b] or both [0Xb] according to CS pin
- WOC_DIFF : Sets the Wake-up On Change based on Δ{sample(t),sample(t-1)}
- EXT_TRIG : Allows external trigger inputs when set, if TRIG_INT_SEL = 0
- TCMP_EN : Enables on-chip sensitivity drift compensation
- BURST_SEL[3:0] : Defines the MDATA in burst mode if SB command argument = 0
- BURST_DATARATE[6:0] : Defines $T_{INTERVAL}$ as BURST_DATA_RATE * 20ms
- OSR2[1:0] : Temperature sensor ADC oversampling ratio
- RES_XYZ[5:0] : Selects the desired 16-bit output value from the 19-bit ADC
- DIG_FILT[1:0] : Digital filter applicable to ADC
- OSR[1:0] : Magnetic sensor ADC oversampling ratio
- SENS_TC_HT[7:0] : Sensitivity drift compensation factor for $T < T_{REF}$
- SENS_TC_LT[7:0] : Sensitivity drift compensation factor for $T > T_{REF}$
- OFFSET_i[15:0] : Constant offset correction, independent for i = X, Y, Z
- WOi_THRESHOLD[15:0] : Wake-up On Change threshold, independent for i = X, Y, Z and T

7.3 Command List

The ST480MC-A only listens to a specific set of commands. Apart from the Reset command, all commands generate a status byte that can be read out. The table below indicates the 12 different commands that are (conditionally) accepted by the ST480MC-A.

CommandName	Symbol	CMD Byte	Output Bytes[2]		
Start Burst Mode	SB	0001 zyxt [1]	N/A		
Start Wake-up on Change Mode	SW	0010 zyxt [1]	N/A		
Start Single Measurement Mode	SM	0011 zyxt[1]	N/A		
Read Measurement	RM	0100 zyxt[1]	N/A		
Read Register	RR	0101 0000	Register Address	High Byte	Low Byte
Write Register	WR	0110 0000	High Byte	Low Byte	Register Address
Exit Mode	EM	1000 0000	N/A		
Memory Recall	HR	1101 0000	N/A		
Memory Store	HS	1110 0000	N/A		
Reset	RT	1111 0000	N/A		

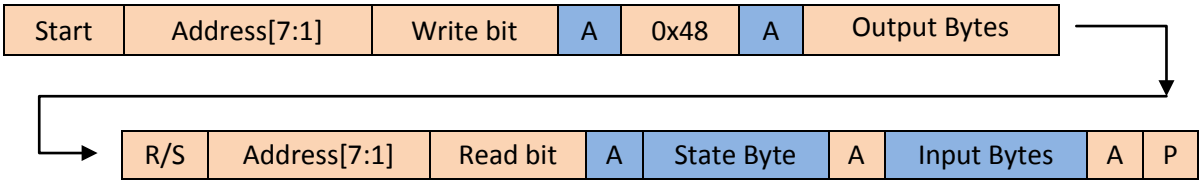
Table 7.2 Command List

Note: (1) The argument in all mode-starting commands (SB/SW/SM) is a nibble specifying the conversions to be performed by the sensor in the following order «zyxt». For example, if only Y axis and temperature are to be measured in Single Measurement mode the correct command to be transmitted is 0x35h.

(2) Output Bytes have to been sent before Start repeat

7.4 Command Usage

All of the command usage should follow the sequence ,Each command has its owns input and output bytes , outputs byte can be found in the command list table , only RR and RM has input bytes.



State Byte:

The status byte is the first byte transmitted by the ST480MC-A in response to a command issued

by the master. It is composed of a fixed combination of informative bits:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BURST_MODE	WOC_MODE	SM_MODE	ERROR	SED	RS	D1	D0

MODE bits

these bits define in which mode the ST480MC-A is currently set. Whenever a mode transition command is rejected, the first status byte after this command will have the expected mode bit cleared, which serves as an indication that the command has been rejected, next to the ERROR bit. The SM_MODE flag can be the result of an SM command or from raising the TRG pin when TRG mode is enabled in the volatile memory of the ST480MC-A.

ERROR bit

this bit is set in case a command has been rejected or in case an uncorrectable error is detected in the memory, a so called ECC_ERROR. A single error in the memory can be corrected (see SED bit), two errors can be detected and will generate the ECC_ERROR. In such a case all commands but the RT (Reset) command will be rejected.

SED bit

the single error detection bit simply flags that a bit error in the non-volatile memory has been corrected. It is purely informative and has no impact on the operation of the ST480MC-A.

RS bit

whenever the ST480MC-A gets out of a reset situation – both hard and soft reset – the RS flag is set to highlight this situation to the master in the first status byte that is read out. As soon as the first status byte is read, the flag is cleared until the next reset occurs.

D[1:0] bits

These bits only have a meaning after the RM commands, when data is expected as a response from the ST480MC-A. The number of response bytes correspond to 2*D[1:0] + 2, so the expected byte counts are either 2, 4, 6 or 8.

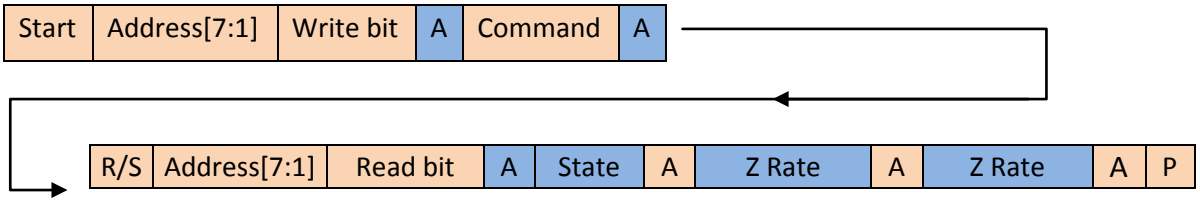
RateByte：

All of the rate byte data is supplied as complement, the bit7 of High Byte is considered to be a sign mark bit

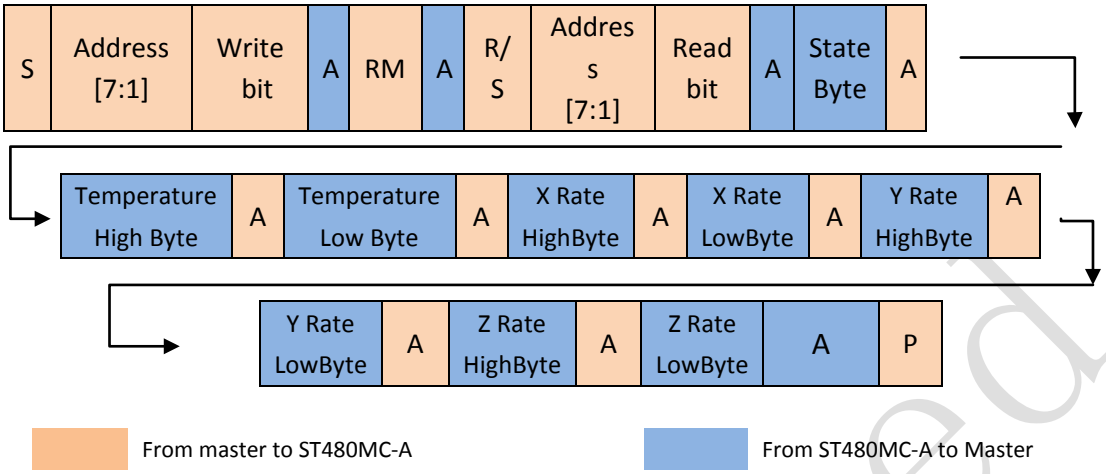
Example of Command usage:

- **Read measurement RM**

The command Read Measurement can get the Sensor Rate while the ST480MC-A set out a int signal, generally speaking, the amounts of input bytes depends on the argument of <zyxt> in mode command , each bit represent two bytes of rate data , the RATA data order is fixed as Temperature Rate, RateX, RateY,RateZ . If we wants RateZ only , the sequence of I2C should follow the rule:

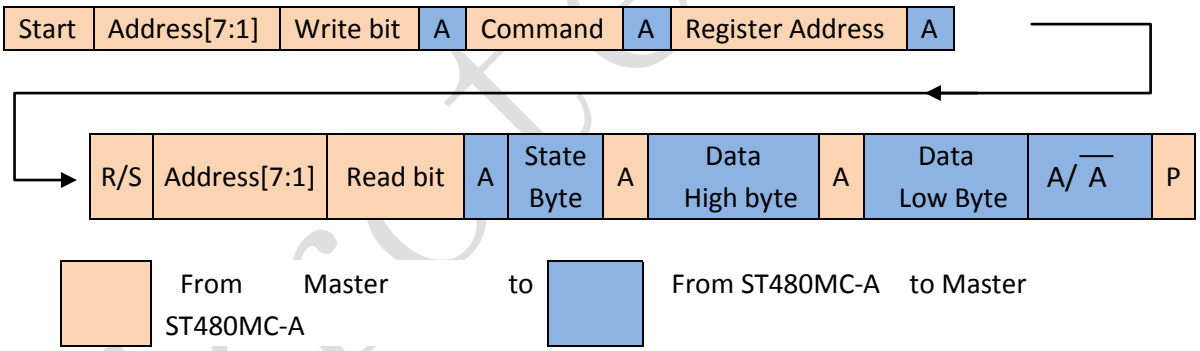


If we want to acquire all of the data, the sequence of I2C should be organized as bellow:



- Read Register(RR)

The Volatile memory data can be read out by the Command of Read Register(RR). The command byte should be followed while the I2C writing address has been sent out. Before a restart of IIC protocol, the register address needed, then the register data will be received following a read IIC address.

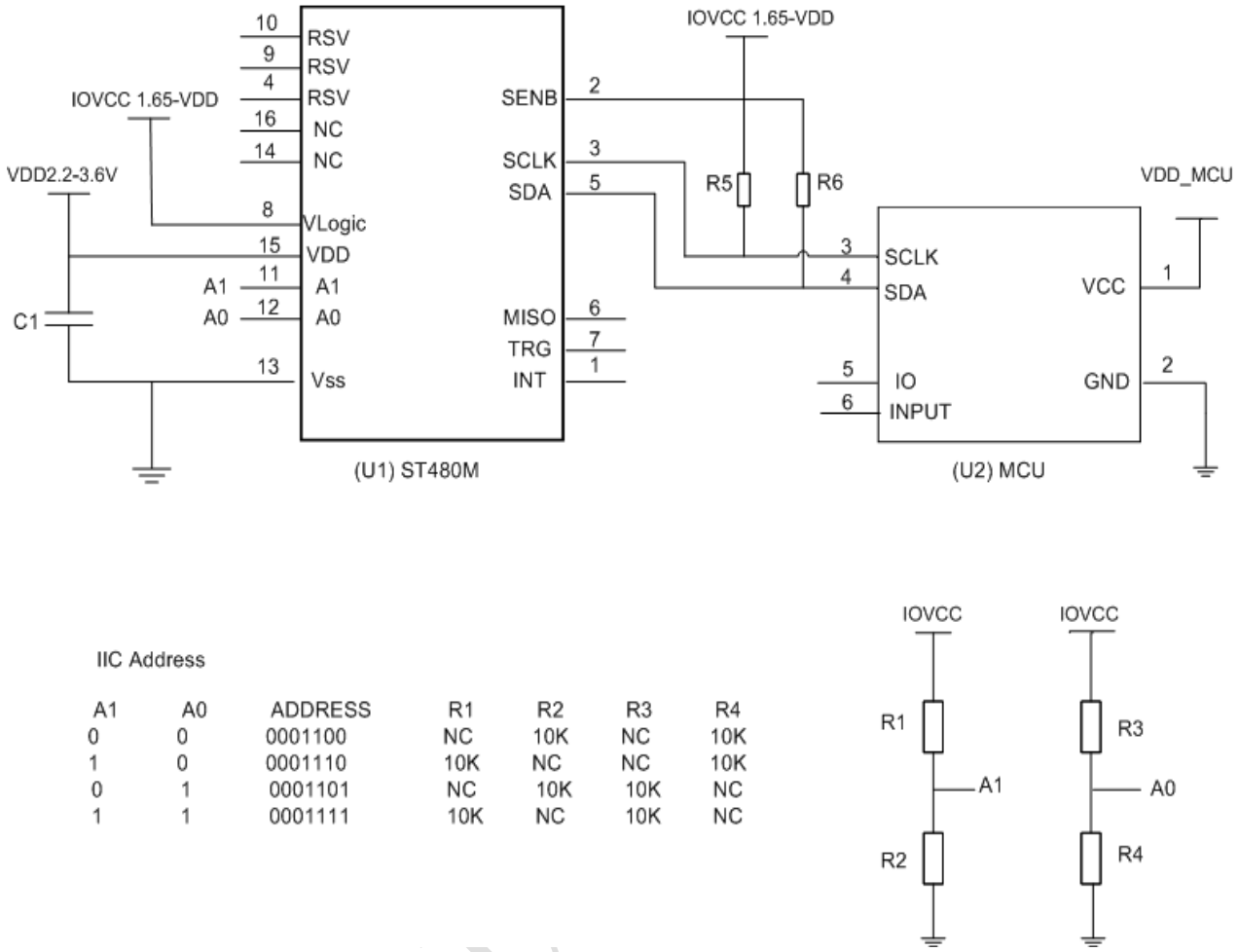


- Other commands

The usage of left commands is quite easy for they do not have input or output bytes, just follow the sequence bellow completely.

8. Typical Application

8.1 Typical Application Circuit



IIC Address

A1	A0	ADDRESS	R1	R2	R3	R4
0	0	0001100	NC	10K	NC	10K
1	0	0001110	10K	NC	NC	10K
0	1	0001101	NC	10K	10K	NC
1	1	0001111	10K	NC	10K	NC

Figure 8.1: Reference Application Circuitry using I2C interface

8.2 Bill of Materials for External Components

Item	Quantity	Reference	Part	Footprint
1	1	C1	0.1uF	SC0603
2	2	R5,R6	2.2Kohm	SR0603
3	4	R1,R2,R3,R4	10Kohm or NC	SR0603
4	1	U1	ST480MC-A	WLCSP-8

9. Package Information

9.1 ST480MC-A WL-CSP 1.28X1.28 Package Outline Dimensions

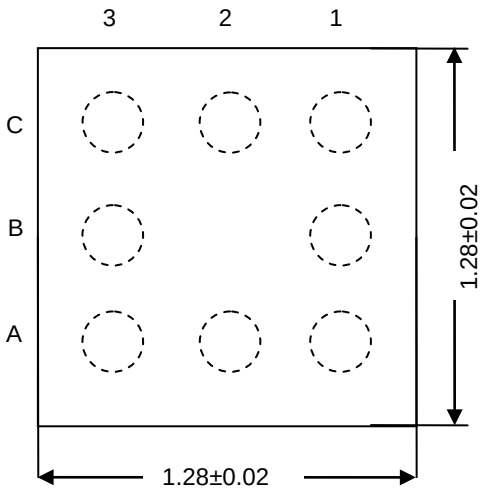


Figure 9.1: Top View (unit mm)

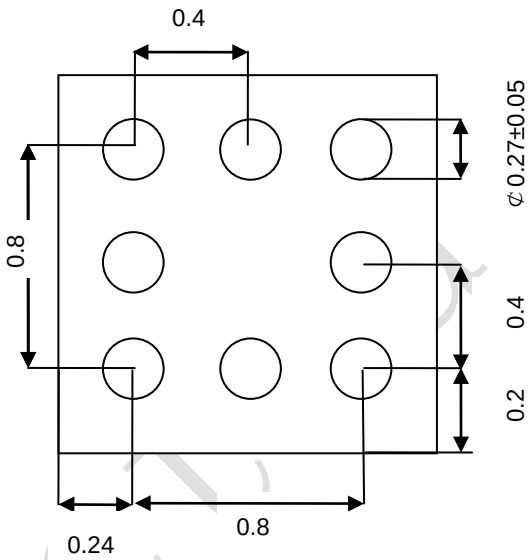


Figure 9.2: Bottom View (unit mm)

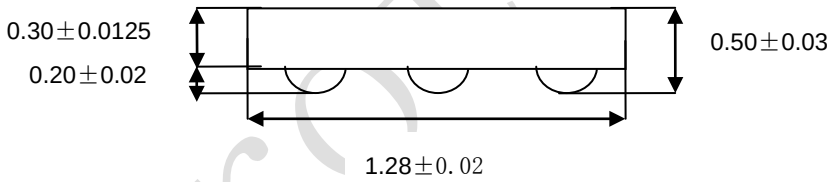


Figure 9.3: Side View (unit mm)

9.2 Recommended Foot Print Pattern

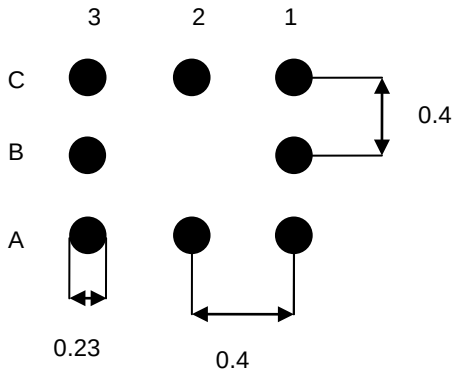


Figure 9.4: Recommended Foot Print Pattern

9.3 Package laser Mark

9.3.1 ST480MC-A marking

Mark	Name	Symbol	Remark
M4C ○	Pin 1 identifier	○	
	Product Name	**M**	Alphabetic M: fixed to identify product name
	Trace Code	**4C**	2 alphanumeric digits, variable to generate mass production trace code: YW (year, week)

9.4 Packing of the Chips

ST480MC-A packing in Tape & Reel (7’’), and meet EIA-481 standard.

9.4.1 Tape size and packing direction:

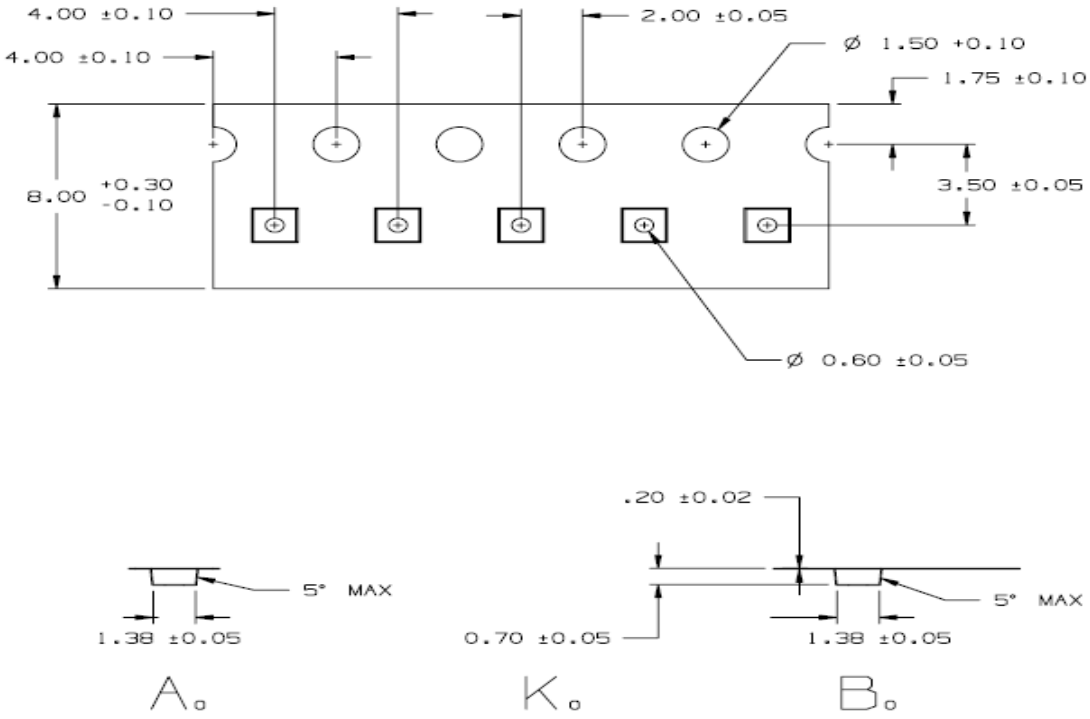


Figure 9.5: Tape size

9.4.2 Packing direction:

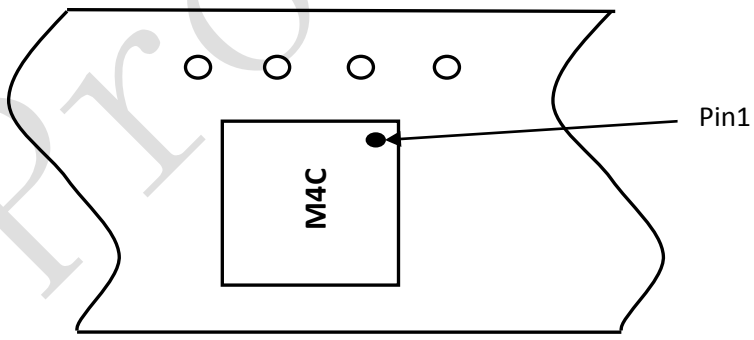


Figure 9.6: Packing direction

9.5 Solder Reflow Curve

Solder Reflow curve follows IPC/JEDEC J-STD-020C Pb-free standards.

9.5.1 Solder Reflow curve

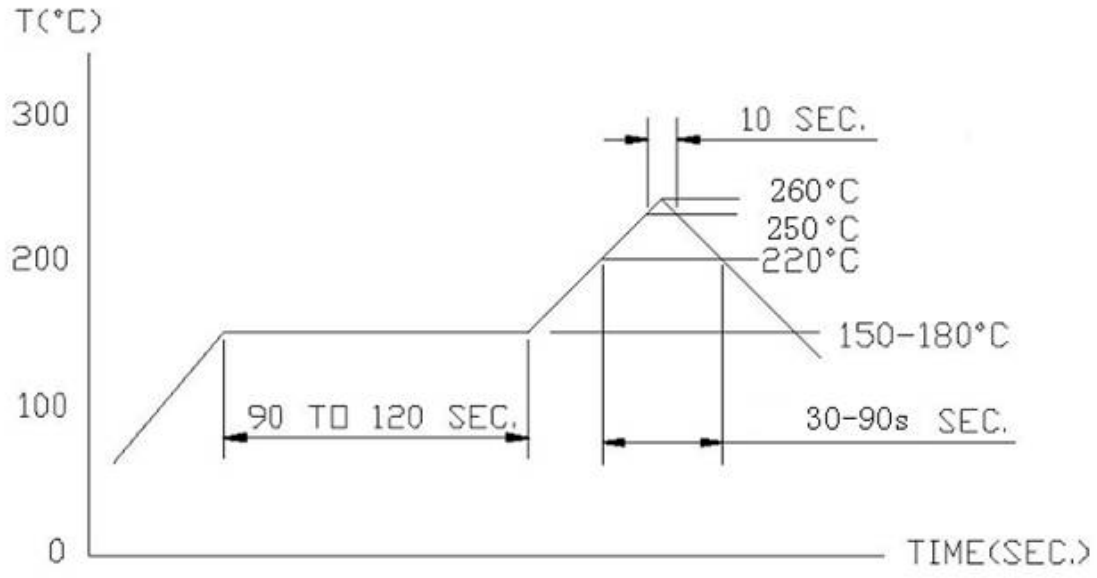


Figure 9.6: Solder Reflow curve

9.5.2 Maintenance temperature is less than 350℃, and duration is less than 30second.

9.6 Storage condition

The storage condition follows JEDEC J-STD-020C, MSL 2.

10. Reliability

ST480MC-A reliability test plan follows JEDEC 47I standards, Stress-Test-Driven Qualification of Integrated Circuits".

11. Environment Compliant

ST480MC-A is compliant with RoHS2.0 standards and meet HF requirements.

12. Revision History

Date	Revision	Changes

2014-6-24	1.0	ST480MC-A initial release
2015-4-9	1.1	Updates
2015-10-26	1.2	Update 9.4.2

13. Disclaimer

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